Design procedure

Line regulation =

Load regulation

=1.6K, so should be at least 80000, which is 98dB

Now, we need to decide which kind of topology we are going to use as an error amplifier to get such a high gain.

The first thing that came across my head is a two-stage amplifier. However, since the two-stage amplifier itself already have two poles, and there is going to have one more pole at the output of the LDO, stability is going to be an issue, and complicated compensation methods will be needed.

So I moved on to a cascoded amplifier. I tried to implement a double-cascoded amplifier in the beginning, but after doing it I could only get 60 dB from it without burning too much power, so I designed a triple-cascoded amplifier to get the gain to be . By this expression, I know that the intrinsic gain for a transistor should be at least 43.

Since I’m triple cascoding transistors, I chose Δ to be 0.1, as small as possible, so that a transistor doesn’t need too much to be in saturation region. By plugging in the intrinsic gain and Δ into the Matlab function, I got the minimum length to be 225 nM. After I got the minimum length, I plugged it into the next Matlab function and got IdW to be 22.3.

To get the width of the transistor, we need to calculate how much current we need. To get the current, we need to get the transconductance To get , we need the unity gain frequency since , and is the of the pass transistor, which is 3.3pF.

The specification required PSR@1MHz to be -20dB, so I decided to make the worst PSR @ ,and I assume that the worst case PSR to be 0dB. Thus, I can approximately get that the should be ten times larger than 1MHz, which is 10MHz. Because ,

=0.207 m=. Thus, , and then I got the width of the NMOS to be 2.1